PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-056570
(43)Date of publication of application : 27.02.2001

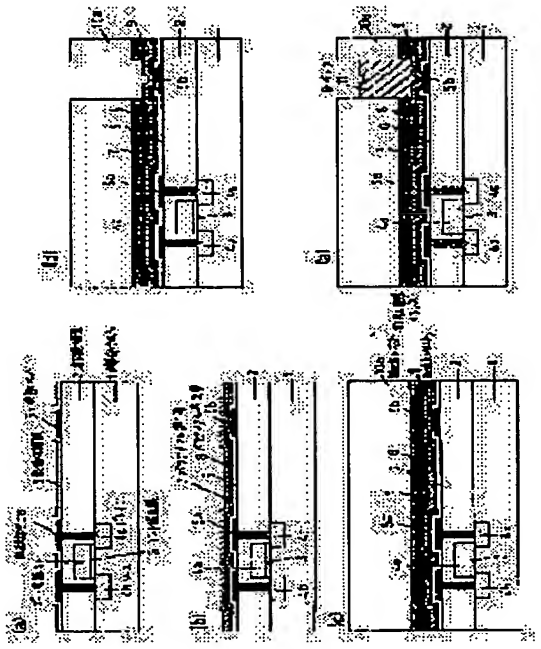
(51)Int.Cl. G03F 7/26
H01L 21/288
H01L 21/027
H01L 21/3205
H01L 21/60

(21)Application number : 11-233694
(22)Date of filing : 20.08.1999

(71)Applicant : MATSUSHITA ELECTRONICS INDUSTRY CORP
(72)Inventor : MATSUMOTO TAKESHI

(54) PRODUCTION OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent the generation of cavities in dents and the resultant formation of resist holes when resists of large film thicknesses are formed in the level difference portions of the dents, etc., on a semiconductor integrated circuit device.
SOLUTION: The narrow dents are formed on the surface of a barrier metal second layer 8 for forming gold bumps 11 between wiring parts 5a of MOS transistors in this process for production. While a wafer 1 is heated, the low- temperature resist 9 is first applied thereon and thereafter, the high-viscosity resist 10a is applied thereon, by which the resist materials are packed into the dents as well. Coverage is thus improved and the generation of the cavities and the resist holes after baking are eliminated. The resist 10 of the large film thickness for forming the selective plating of the gold bumps may be assured by the high-viscosity resist 10a.



LEGAL STATUS

[Date of request for examination] 01.08.2002
[Date of sending the examiner's decision of rejection] 22.11.2005
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]